10/048192 ,060302

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SUBSTITUTE FORM PTO-1390 U S DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER
12816-042001

U.S. APPLICATION NO. (If Known, see 37 CFR 1.5)
10/048192

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE00/02555	27 July 2000	27 July 1999

TITLE OF INVENTION
METHOD FOR PRODUCING A SEMICONDUCTOR MEMORY ELEMENT

APPLICANT(S) FOR DO/EO/US
Volker Weinrich and Manfred Engelhardt

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☐ This is an express request to promptly begin national examination procedures (35 U.S.C. 371(f)).
4. ☐ The US has been elected by the expiration of 19 months from the priority date (PCT Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is attached hereto (required only if not communicated by the International Bureau).
   b. ☐ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
8. ☐ An English language translation of amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11 to 16 below concern other documents or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☐ A substitute specification.
15. ☐ A change of power of attorney and/or address letter.
16. ☒ Other items or information:
    ☒ International Search Report
    ☒ International Preliminary Examination Report
    ☐
    ☐
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Leroy Jenkins — Typed Name of Person Signing

U.S. APPLICATION NO. (IF KNOWN)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
10/048192	PCT/DE00/02555	12816-042001

17. ☒ The following fees are submitted:

Basic National Fee (37 CFR 1.492(a)(1)- (5)):

Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO..... **$1040**

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890**

International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740**

International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710**

International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4) **$100**

CALCULATIONS PTO USE ONLY	
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Claims	Number Filed	Number Extra	Rate		
Total Claims	20 - 20 =		x **$18**	$0.00	
Independent Claims	3 - 3 =		x **$84**	$0.00	
MULTIPLE DEPENDENT CLAIMS(S) (if applicable)			+ **$280**	$0.00	
TOTAL OF ABOVE CALCULATIONS =				$890.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$0.00	
SUBTOTAL =				$890.00	
Processing fee of **$130** for furnishing the English Translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f))				$0.00	
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Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property +				$0.00	
TOTAL FEES ENCLOSED =				$890.00	
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a. ☒ A check in the amount of $890.00 to cover the above fees is enclosed.
b. ☐ Please charge my Deposit Account No. 06-1050 in the amount of $0.00 to cover the above fees. A duplicate copy of this sheet is enclosed.
c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 06-1050. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b) must be filed and granted to restore the application to pending status.

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44,381
REGISTRATION NUMBER

Attorney's Docket No.: 12816-042001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: Engelhardt, M., et al.	Art Unit	: Unknown
Serial No.	: To Be Assigned	Examiner	: Unknown
Filed	: Herewith		
Title	: METHOD FOR PRODUCING A SEMICONDUCTOR MEMORY ELEMENT		

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Prior to examination, please amend the application as follows:

In the claims:

Amend claims 1-6 as follows:

1. (Once amended) A method for fabricating a contact hole for a semiconductor memory component, having a silicon substrate, an intermediate dielectric layer arranged on said substrate, and an upper layer arranged on said intermediate dielectric layer, the method comprising:

forming a perforated mask on the upper layer, the mask including a material which exhibits temperature stability during a later deposition process;

etching the upper layer and a depression into the intermediate dielectric layer as far as a residual thickness using the perforated mask;

depositing a layer including O_3/TEOS-SiO_2 onto a structure thus obtained including the perforated mask;

removing the layer including O_3/TEOS-SiO_2 from a bottom of the depression by etching; and

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Leroy Jenkins
Typed or Printed Name of Person Signing Certificate

thereupon lowering the depression by etching in order to produce the contact hole as far as an interface with the silicon substrate, the silicon substrate being uncovered, the layer including O_3/TEOS-SiO_2 serving as a lateral seal of the upper layer during the lowering of the depression.

2. (Once amended) The method as claimed in claim 1, wherein forming the perforated mask comprises forming a perforated mask including polyimide.

3. (Once amended) The method as claimed in claim 1, wherein forming the perforated mask comprises forming a perforated mask including photoimide.

4. (Once amended) The method as claimed in claim 1, wherein, after the uncovering of the silicon substrate at the bottom of the contact hole, the silicon substrate being spared, a second layer including O_3/TEOS-SiO_2 is deposited into the contact hole and onto a top surface proximate the contact hole.

5. (Once amended) The method as claimed in claim 4, wherein the perforated mask material is stripped prior to deposition of the second layer including O_3/TEOS-SiO_2.

6. (Once amended) The method as claimed in claim 1, further comprising:

selecting a material for the upper layer from the group consisting of a ferroelectric material and a material having a high dielectric constant.

Please add new claims 7 – 20.

--7. (New) The method of claim 6, wherein selecting the material includes selecting a material from the group consisting of strontium bismuth tantalate, PZT, and barium strontium titanate.

8. (New) A method for fabricating a contact hole for a semiconductor component, the method comprising:

providing a silicon substrate including an intermediate dielectric layer formed thereon;

forming a resist mask over the intermediate dielectric layer, the resist mask defining an opening;

etching the intermediate dielectric layer through the resist mask opening to form a depression having sidewalls, leaving a residual thickness of the intermediate dielectric layer at a bottom portion of the depression;

depositing a layer including O_3/TEOS-SiO_2 over the intermediate dielectric layer and along the sidewalls of the depression;

etching the layer including O_3/TEOS-SiO_2 from the bottom of the depression; and

further etching the intermediate dielectric layer to extend the depression further down to an interface between the intermediate dielectric layer and the silicon substrate until a top surface of the silicon substrate is uncovered.

9. (New) The method of claim 8, wherein providing a silicon substrate includes providing a silicon substrate having an upper layer disposed over the intermediate dielectric layer, the method further comprising:

prior to etching the intermediate dielectric layer, forming the resist mask on the upper layer; and

etching a portion of the upper layer through the resist mask opening.

10. (New) The method of claim 9, wherein providing a silicon substrate comprises providing a silicon substrate having an upper layer including a ferroelectric material.

11. (New) The method of claim 10, wherein providing a silicon substrate comprises providing a silicon substrate having an upper layer including strontium bismuth tantalate.

12. (New) The method of claim 9, wherein providing a silicon substrate comprises providing a silicon substrate having an upper layer including a material with a high dielectric constant.

13. (New) The method of claim 12, wherein providing a silicon substrate comprises providing a silicon substrate having an upper layer including barium strontium titanate.

14. (New) The method of claim 13, further comprising:

after etching the intermediate dielectric to extend the depression until the top surface of silicon is uncovered, depositing a second layer having O_3/TEOS-SiO_2 into the depression and onto a top surface proximate to the depression.

15. (New) The method of claim 14, further comprising:

stripping the resist mask before depositing the second layer.

16. (New) A method for forming a contact hole, the method comprising:

applying a mask over an intermediate layer formed over a substrate, the mask defining an opening;

forming a depression in the intermediate layer through the opening, the depression having sidewalls and a bottom portion;

forming a protective layer on the sidewalls of the depression; and

further deepening the depression.

17. (New) The method of claim 16, further comprising selecting the protective layer to include an oxide.

18. (New) The method of claim 17, further comprising selecting the protective layer to include silicon dioxide.

19. (New) The method of claim 16, wherein forming a depression comprises etching the intermediate layer.

20. (New) The method of claim 16, further comprising selecting the intermediate layer to include a dielectric material.--

In the abstract:

Replace the abstract with the following version.

A method for fabricating a contact hole for a semiconductor memory element. The memory element includes a silicon substrate, an intermediate dielectric layer on the substrate, and an upper layer on the intermediate dielectric layer. The method includes forming a perforated mask on the upper layer, the mask including a material that exhibits temperature stability. The upper layer and a depression are etched into the intermediate dielectric layer as far as a residual thickness using the perforated mask. A layer including O_3/TEOS-SiO_2 is deposited onto a structure thus obtained. The layer including O_3/TEOS-SiO_2 is removed from a bottom of the depression by etching. The depression is lowered by etching to produce the contact hole as far as an interface with the silicon substrate, the silicon substrate being uncovered, and the layer including O_3/TEOS-SiO_2 serving as a lateral seal of the upper layer during the lowering of the depression.

Applicant : Engelhardt, M., et al.
Serial No. : To Be Assigned
Filed : Herewith
Page : 6

Attorney's Docket No.: 12816-042001

REMARKS

Claims 1-6 have been amended to conform to U.S. practice and to eliminate multiple dependent claims. New claims 7-20 have been added.

Now pending in this application are claims 1-7, 8-15, and 16-20. Of these, claims 1, 8, and 16 are independent.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be examined. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: Jan. 25, 2002

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Version with markings to show changes made

In the claims:

Claims 1-6 have been amended as follows:

1. (Once amended) A method for fabricating a contact hole for a semiconductor memory component, [in particular a DRAM or an FRAM], having a silicon substrate, an intermediate dielectric layer [(1)] arranged on said substrate, and an upper layer [(3) made of a ferroelectric material or made of a material having a high dielectric constant being] arranged on said intermediate dielectric layer, [having the steps of] the method comprising:

f[F]orming a perforated mask on the upper layer [(3)], the mask including a material which exhibits temperature stability during a later deposition process [being used for the perforated mask];

e[E]tching the upper layer [(3)] and a depression [(8')] into the intermediate dielectric layer [(1)] as far as a residual thickness [(d_0)] using the perforated mask;

d[D]epositing a layer [made of] including O_3/TEOS-SiO_2 onto [the] a structure thus obtained including the perforated mask [in the later deposition process];

r[R]emoving the layer [made of] including O_3/TEOS-SiO_2 from [the] a bottom of the depression [(8')] by etching; and

t[T]hereupon lowering the depression [(8')] by etching in order to produce the contact hole as far as [the] an interface with the silicon substrate, the [latter] silicon substrate being uncovered, the layer [made of] including O_3/TEOS-SiO_2 serving as a lateral seal of the upper layer [(3)] during the [etching process] lowering of the depression.

2. (Once amended) The method as claimed in claim 1, wherein [polyimide is used as the material for] forming the perforated mask comprises forming a perforated mask including polyimide.

3. (Once amended) The method as claimed in claim 1, wherein [photoimide is used as the material for] forming the perforated mask comprises forming a perforated mask including photoimide.

4. (Once amended) The method as claimed in claim 1, [2 or 3,] wherein, after the uncovering of the silicon substrate [in the region of] at the bottom of the contact hole, the [latter] silicon substrate being spared, a second layer [made of] including O_3/TEOS-SiO_2 is [again] deposited [onto this structure] into the contact hole and onto a top surface proximate the contact hole.

5. (Once amended) The method as claimed in claim 4, wherein the perforated mask material is stripped prior to [renewed] deposition of the second layer including O_3/TEOS-SiO_2.

6. (Once amended) The method as claimed in claim 1, [one of the preceding claims, wherein a layer made of] further comprising:

selecting a material for the upper layer from the group consisting of a ferroelectric material [, in particular SBT or PZT, or made of a] and a material having a high dielectric constant[, in particular BST, is used as the upper layer (3)].

In the abstract:

[The invention relates to a method for producing a semiconductor memory element, in particular a DRAM or FRAM. Said memory element comprises a silicon substrate, an intermediate oxide layer (1) applied to the latter, upon which an upper layer (3) consisting of a ferroelectric material or a material with higher dielectric constants is provided. A contact cavity (8) which extends up to the border between the silicon substrate and the upper layer is etched, from the starting point of an opening (5) in a cavity mask which has been configured in a previous stage. A material resistant to high temperatures is used for the cavity mask. Such a material must withstand high temperatures so that the subsequent deposition of O_3-TEOS-SiO_2 onto this layer (for example polymide) can take place, without causing any degradation of said layer. The cavity mask is used for etching into the intermediate oxide layer (1), causing the

formation of a recess (8'). A layer consisting of O_3-TEOS-SiO_2 is then deposited onto the resultant structure. In order to create the contact cavity, the O_3-TEOS-SiO_2 layer is removed from the base of the recess (8') by etching and said recess (8') is then sunk to the border with the silicon substrate by etching, thus exposing the substrate.]

A method for fabricating a contact hole for a semiconductor memory element. The memory element includes a silicon substrate, an intermediate dielectric layer on the substrate, and an upper layer on the intermediate dielectric layer. The method includes forming a perforated mask on the upper layer, the mask including a material that exhibits temperature stability. The upper layer and a depression are etched into the intermediate dielectric layer as far as a residual thickness using the perforated mask. A layer including O_3/TEOS-SiO_2 is deposited onto a structure thus obtained. The layer including O_3/TEOS-SiO_2 is removed from a bottom of the depression by etching. The depression is lowered by etching to produce the contact hole as far as an interface with the silicon substrate, the silicon substrate being uncovered, and the layer including O_3/TEOS-SiO_2 serving as a lateral seal of the upper layer during the lowering of the depression.

2/pats

Description

Method for fabricating a semiconductor memory component

The invention relates to a method for fabricating a contact hole for a semiconductor memory component, in particular a DRAM or an FRAM, having a silicon substrate, an intermediate dielectric layer arranged on said substrate, an upper layer made of a ferroelectric material or made of a material having a high dielectric constant being arranged on said intermediate dielectric layer.

Depending on the chip design or the chip layout, it is necessary, in a large scale integrated DRAM or FRAM, when using materials having a high dielectric constant, for example BST (BST stands for Barium Strontium Titanate), and ferroelectric materials, for example SBT (SBT stands for Strontium Bismuth Tantalate), to etch through these materials during the plasma etching of the contact hole to the silicon substrate. In this case, contamination of the monocrystalline silicon substrate which is uncovered at the bottom of the contact hole must be avoided in order to prevent an adverse effect on the selection transistor of DRAM or FRAM.

For this purpose, it is known to carry out two lithography process steps or two lithography levels. In this case, in the first lithography process step, a window is produced in the ferroelectric layer by plasma etching using a resist mask. In the second lithography process step, the actual contact hole is thereupon etched down to the silicon substrate using a new, smaller resist mask. Although this conventional method leads to the aim of avoiding contamination of the bottom of the contact hole, it is nonetheless very complex on account of the use of two lithography process steps or lithography levels.

DE 43 40 419 C2 discloses a method for fabricating a semiconductor device having an insulating layer in which a contact hole is formed. In this known method, a photoresist perforated mask is formed on the insulating layer and anisotropic etching is carried out to form part of the contact hole whilst leaving a residual layer thickness of the insulating layer. Furthermore, the photoresist mask is removed and a TEOS layer is deposited on the resulting structure. The TEOS layer is then etched anisotropically in order to remove the TEOS layer at the bottom of the partial contact hole. Afterward, the contact hole is completed by means of an etching process, the contact hole having a configuration in which the opening diameter increases through the upward direction.

DE 195 28 746 C1 discloses a method for producing a silicon dioxide layer on surface sections of a structure with sidewall sections and a bottom section.

Accordingly, an object of the present invention consists in providing a method of the type mentioned in the introduction which leads to the aim with a simplified, i.e. a single, lithography process.

This object is achieved by the subject matter of claim 1. Advantageous developments of the invention are specified in the subclaims.

In other words, the method according to the invention is based on the use of an organic mask layer which is stable at high temperatures, preferably made of polyimide or photoimide and on the partial etching of the dielectric material layer (intermediate oxide) in combination with the etching-through of the overlying layer made of the material having a high dielectric constant or the ferroelectric material. A depression is thereby achieved in the dielectric layer, except for a

residual layer thickness which is less than or equal to the residual thickness of the mask layer after the etching step.

According to the invention, the depression is thereupon sealed laterally by conformal deposition of a layer made of O_3/TEOS-SiO_2 (TEOS stands for tetraethyl orthosilicate). The process temperature required in this case is typically 400°C and is tolerated by the perforated mask layer which is stable at high temperatures, without degradation effects.

An oxide etching thereupon uncovers the bottom of the depression in a manner similar to that in the case of a spacer etching, said bottom thereupon being lowered down to the bottom of the contact hole by etching.

The organic layer furthermore serves as a perforated mask and is subsequently removed.

This is advantageously followed by selective renewed deposition of O_3/TEOS-SiO_2 for the purpose of sealing exclusively the lateral wall of the contact hole and the surface of the wafer, with the bottom of the contact hole being spared. This is followed, in a manner known per se, by contact hole aftertreatment for removing silicon substrate material that is possibly damaged, and metallization of the contact hole.

The method according to the invention thus proceeds more simply than the conventional method with regard to the lithography process.

The invention is explained in more detail below by way of example using exemplary embodiments with reference to the drawings.

In the figures:

Figures 1A to 1D diagrammatically show the sequence of steps of a conventional method for fabricating a semiconductor memory component using materials having a high dielectric constant and ferroelectric materials, and

Figures 2A to 2G diagrammatically show the sequence of steps of a method according to the invention for fabricating a semiconductor memory component using materials having a high dielectric constant and ferroelectric materials.

In order to provide a better understanding of the invention, firstly an explanation will be given, with reference to Figures 1A to 1D, of a conventional method for fabricating a semiconductor memory component using materials having a high dielectric constant and ferroelectric materials. This conventional method requires the use of two lithography levels or lithography steps.

The first lithography level is shown in Figures 1A and 1B, and the second lithography level is shown in Figures 1C and 1D. In accordance with these figures, the semiconductor memory element is constructed from a silicon substrate 11, whose exact structure is not shown, and on which a dielectric layer 1 is arranged, the underside of which adjoins the top side of the silicon substrate 11. This boundary layer is designated generally by the reference numeral 2 in Figures 1A to 1D.

The top side of the dielectric layer 1 is adjoined by a continuous layer - in Figure 1A - having a high dielectric constant (or a ferroelectric layer), which is generally designated by the reference numeral 3. The layer 3 is composed, for example, of BST (BST stands

for Barium Strontium Titanate). A ferroelectric layer 3, by contrast, is composed, for example, of SBT (SBT stands for Strontium Bismuth Tantalate).

The top side of the layer 3 having a high dielectric constant is firstly covered completely by a resist layer 4. This resist layer 4 is converted, in a known manner, into a resist mask (perforated mask 4) having a multiplicity of openings 5. The opening 5 serves for etching a window 6 into the layer 3 having a high dielectric constant, as shown in Figure 1B, which already shows the result of the next method step resulting in the removal of the resist layer 4. This resist removal step is also known as resist stripping.

As shown in Figure 1C, a resist layer is again applied to the surface structure of Figure 1B, which resist layer is generally designated by the reference numeral 7 and is converted, in a known manner, into a resist mask having perforations at the locations at which a contact hole is intended to be introduced into the dielectric layer 1. This contact hole is produced by means of the second lithography level by etching the dielectric layer 1 with the aid of the resist mask as far as the boundary layer 2, as shown in Figure 1D, which already illustrates the result of the next step according to which the resist layer 7 is completely removed.

The etching steps explained above usually involve plasma etching.

The contact hole, which is generally designated by the reference numeral 8, has a typical structural size or a diameter d_1 of 0.6 µm and is thus approximately half as large as the window 6 having the diameter d_2. These dimensions are not obligatory, however, but rather are chosen only by way of example.

What is achieved by the method steps expressed in Figures 1A to 1D is that the bottom of the contact hole 8 (Figure 1D), i.e. that surface of the monocrystalline silicon substrate (boundary area 2) which is uncovered by this contact hole, is not contaminated. In the case of a direct etching (i.e. when using a single lithography mask) as far as the Si, the plasma would be contaminated, and thus so, too, would the monocrystalline silicon substrate. In order to prevent an adverse effect on the functioning of the semiconductor memory component, the silicon substrate must not be contaminated.

The method according to the invention for fabricating the semiconductor memory component under discussion will now be explained with reference to Figures 2A to 2G. The method according to the invention differs from the method explained above with reference to Figures 1A to 1D by the fact that one lithography level or one lithography step is obviated. Accordingly, the method according to the invention is based on a single lithography level.

Insofar as the structure shown in Figures 2A to 2G corresponds to that of Figures 1A to 1D, the same reference numerals are used.

Figure 2A corresponds to Figure 1A with the difference that, in the method step shown in Figure 2A, a mask made of conventional resist is not used, rather a mask - generally designated by 4' - made of an organic material, such as, for instance, polyimide or photoimide, is used, the mask material being stable relative to a layer made of O_3/TEOS-SiO_2 which is deposited in the later method step in accordance with Figure 2C.

The method step shown in Figure 2A is followed by the method step shown in Figure 2B, which, using the

opening 5, implements the etching both of the layer 3 having a high dielectric constant and of a depression 8' into the dielectric layer 1, which can also be referred to as partial etching in the sense of the contact hole 8 of Figure 1D. In the etching step shown in Figure 2B, the mask layer 4' is additionally removed to an extent such that a mask layer thickness d_p remains, which is greater than the residual thickness d_0 between the bottom of the depression 8' and the interface 2 with the silicon substrate. For the subsequent process steps, it is essential that the perforated mask residual thickness d_p be greater than or equal to the dielectric residual thickness d_0: $d_p \geq d_0$. However, this last is not absolutely necessary, but rather only by way of example. What is essential is that the selectivity of the subsequent etching step allows d_0 to be etched with a mask of thickness d_p.

In the next process step, shown in Figure 2C, a layer made of O_3/TEOS-SiO_2 is deposited onto the structure of Figure 2B in a highly conformal manner, which layer also lines the depression 8'. This layer is designated by the reference numeral 9. The purpose of the layer 9 is to laterally seal the layer 3 having a high dielectric constant in the region 6' and the dielectric layer 1 in the region of the depression walls. The process temperature during the deposition of the layer 9 is typically 400°C and is tolerated by the layer 4' which is stable at high temperatures, without degradation effects.

As illustrated in Figure 2D, the next process step that follows is renewed etching similar to that in the case of a spacer etching for the purpose of uncovering the top side of the perforated mask layer 4' and also the bottom of the depression 8'. The upper edge of the hole in the layer 4' is also shortened during this etching process. As shown in Figure 2E, this etching process is continued until the bottom of the depression 8' has

reached the interface 2 with the silicon substrate. Afterward, as shown in Figure 2F, the layer 4' is removed (stripping).

Afterward, O_3/TEOS-SiO_2 is deposited selectively again, as is shown in Figure 2G and designated by the reference numeral 10. This selective O_3/TEOS-SiO_2 deposition is explained in detail in German Patent No. 19 528 746, according to which exclusively the top side of the layer 3 having a high dielectric constant and the side wall of the contact hole 8 are coated, whereas no deposition whatsoever is effected at the bottom of the contact hole 8. This is followed by a process step (not illustrated) according to which the contact hole 8 is subjected to an aftertreatment in order to remove possibly damaged material of the silicon substrate at the bottom of the contact hole and to metallize the contact hole.

The method according to the invention as shown in Figures 2A to 2G accordingly allows, in a single lithography level, the introduction of a contact hole without contamination of the monocrystalline silicon substrate at the bottom of the contact hole.

Patent Claims

1. A method for fabricating a contact hole for a semiconductor memory component, in particular a DRAM or an FRAM, having a silicon substrate, an intermediate dielectric layer (1) arranged on said substrate, an upper layer (3) made of a ferroelectric material or made of a material having a high dielectric constant being arranged on said intermediate dielectric layer, having the steps of:

Forming a perforated mask on the upper layer (3), a material which exhibits temperature stability during a later deposition process being used for the perforated mask;

Etching the upper layer (3) and a depression (8') into the intermediate dielectric layer (1) as far as a residual thickness (d_0) using the perforated mask;

Depositing a layer made of O_3/TEOS-SiO_2 onto the structure thus obtained including the perforated mask in the later deposition process;

Removing the layer made of O_3/TEOS-SiO_2 from the bottom of the depression (8') by etching; and

Thereupon lowering the depression (8') by etching in order to produce the contact hole as far as the interface with the silicon substrate, the latter being uncovered, the layer made of O_3/TEOS-SiO_2 serving as a lateral seal of the upper layer (3) during the etching process.

2. The method as claimed in claim 1, wherein polyimide is used as the material for the perforated mask.

3. The method as claimed in claim 1, wherein photoimide is used as the material for the perforated mask.

4. The method as claimed in claim 1, 2 or 3, wherein, after the uncovering of the silicon substrate in the region of the bottom of the contact hole, the latter being spared, a layer made of O_3/TEOS-SiO_2 is again deposited onto this structure.

5. The method as claimed in claim 4, wherein the perforated mask material is stripped prior to renewed deposition of O_3/TEOS-SiO_2.

6. The method as claimed in one of the preceding claims, wherein a layer made of a ferroelectric material, in particular SBT or PZT, or made of a material having a high dielectric constant, in particular BST, is used as the upper layer (3).

Abstract

The invention provides a method for fabricating a semiconductor memory component, in particular a DRAM or FRAM, having a silicon substrate, an intermediate oxide layer (1) arranged on said substrate, an upper layer (3) made of a ferroelectric material or made of a material having a high dielectric constant being arranged on said intermediate oxide layer, a contact hole (8) extending as far as the interface between the silicon substrate and the upper layer being introduced by means of etching proceeding from an opening (5) in a perforated mask, which was formed in a preceding step. For the perforated mask, use is made of a material which is stable at high temperatures, to be precise stable at high temperatures so that O_3/TEOS-SiO_2 can subsequently be deposited onto this layer (e.g. polyimide) without degradation of this layer. The etching is performed using the perforated mask into the intermediate oxide layer (1) to form a depression (8'). A layer made of O_3/TEOS-SiO_2 is deposited onto the structure thus obtained. The layer made of O_3/TEOS-SiO_2 is removed from the bottom of the depression (8') by etching, and the depression (8') is thereupon lowered by etching in order to produce the contact hole as far as the interface with the silicon substrate, the latter being uncovered.

(Figure 2G)

FIG 1D

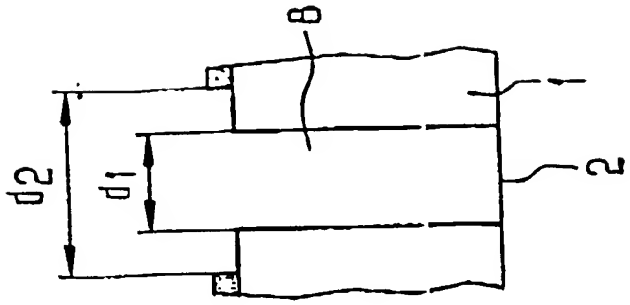


FIG 1C

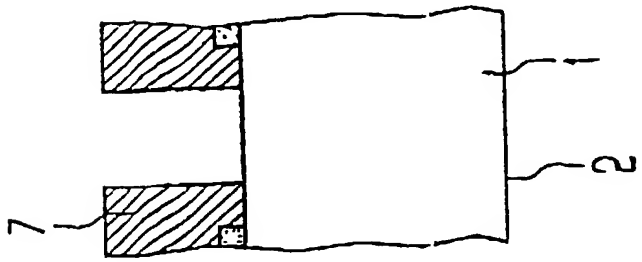


FIG 1B

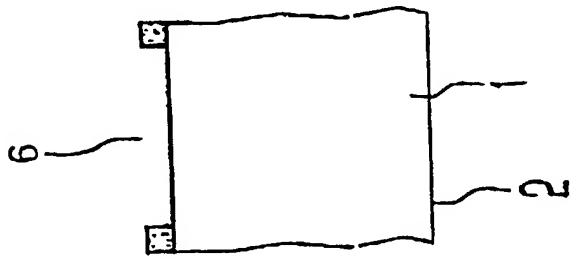


FIG 1A

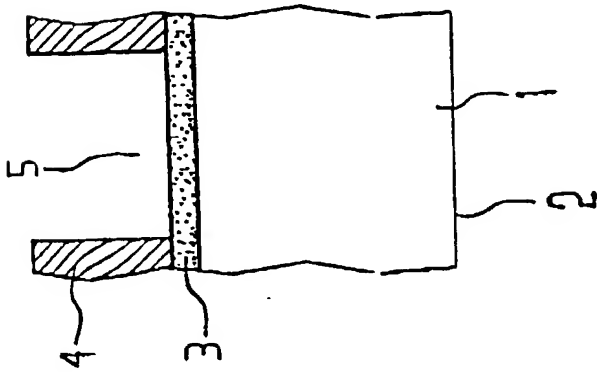


FIG 2A

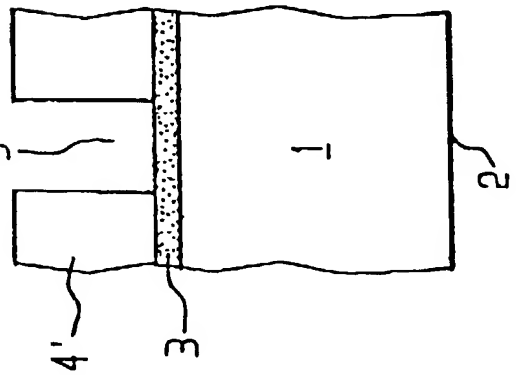


FIG 2B

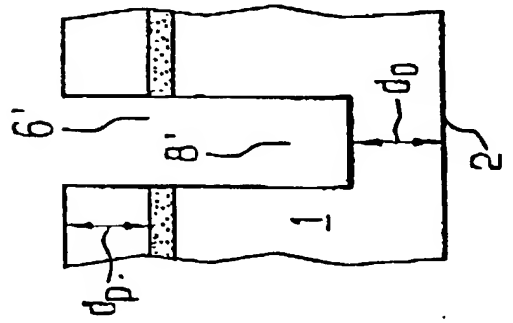


FIG 2C

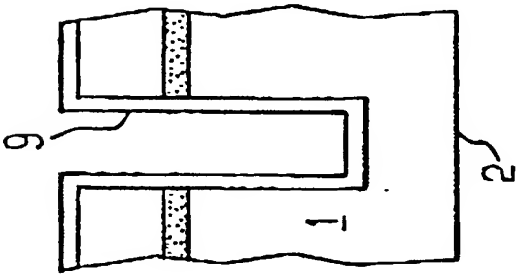


FIG 2D

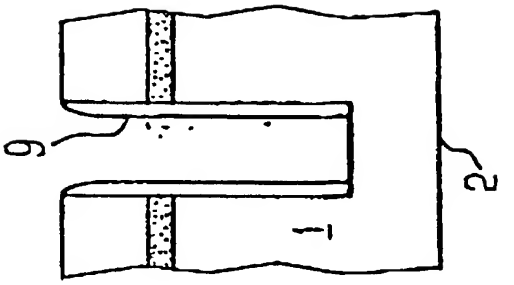


FIG 2E

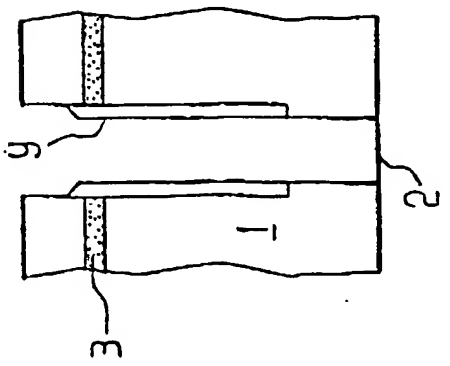


FIG 2F

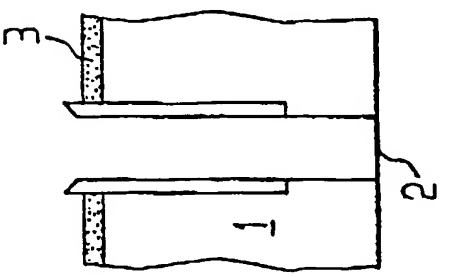
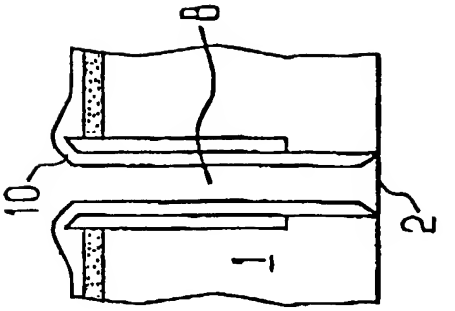


FIG 2G



Attorney's Docket No.: 12816-042001
Client's Ref. No.: S 1556 SB/pra

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled METHOD FOR PRODUCING A SEMICONDUCTOR MEMORY ELEMENT, the specification of which:

[] is attached hereto.
[X] was filed on January 25, 2002 as Application Serial No. 10/048,192 and was amended on _____.
[X] was described and claimed in PCT International Application No. PCT/DE00/02555 filed on 07/27/2000 and as amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Country	Application No.	Filing Date	Priority Claimed
Germany	199.35.130.9	July 27, 1999	[X] Yes [] No

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patents issued thereon.

Attorney's Docket No.: 12816-042001
Client's Ref. No.: S 1556 SB/pra

Combined Declaration and Power of Attorney

1-00

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2-00

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